WHAT IS CLAIMED IS:

1. A differential signal output apparatus comprising:

a differential pair for receiving differential signals;

a current source, connected to one end of the differential pair, for supplying a current to the differential pair; and

a capacitor connected between a branching node for branching from the current source to transistors and a low impedance node.

2. The differential signal output apparatus, as claimed in Claim 1, wherein:

the low impedance node is a power supply voltage or a ground voltage.

3. A differential signal output apparatus comprising:

a differential pair for receiving differential signals;

a first current source, connected to one end of the differential pair, for supplying a current to the differential pair; and

a capacitor connected between a branching node for branching from the first current source to transistors and a current supply unit.

4. The differential signal output apparatus, as claimed in Claim 3, wherein:

the current supply circuit is a second current source.

5. The differential signal output apparatus, as claimed in Claim 4, comprising:

a first differential pair constituted of a first conductivity type;

a first current source, connected to one end of the first differential pair, for supplying a current to the first differential pair;

a second differential pair of which differential output terminals are connected to the differential output terminals of the first differential pair, being constituted of a second conductivity type;

a second current source connected to one end of the second differential pair, for supplying a current to the second differential pair; and

a capacitor connected between a first branching node for branching from the first current source to the transistors of the first conductivity

type and a second branching node for branching from the second current source to the transistors of the second conductivity type.

6. The differential signal output apparatus, as claimed in Claim 1, wherein:

the capacitor forms a current path for letting the current supplied from the current source flow when the current to the differential pair is cut off.

7. The differential signal output apparatus, as claimed in Claim 3, wherein:

the capacitor forms a current path for letting the current supplied from the first current source flow when the current to the differential pair is cut off.

8. A differential signal output apparatus comprising:

a differential pair for receiving differential signals;

a current source, connected to one end of the differential pair, for supplying a current to the differential pair; and

a transitional response circuit for forming a current path for letting the current supplied from the current source flow when the current to the differential pair is cut off.

9. The differential signal output apparatus, as claimed in Claim 8, wherein:

the transitional response circuit is a capacitor.

10. The differential signal output apparatus, as claimed in Claim 6, wherein:

the impedance of the capacitor is smaller than the load impedance in the differential signal output apparatus at a transitional response frequency at which a transitional current flows to the capacitor.

11. The differential signal output apparatus, as claimed in Claim 7, wherein:

the impedance of the capacitor is smaller than the load impedance in the differential signal output apparatus at a transitional response frequency at which a transitional current flows to the capacitor.

12. The differential signal output apparatus, as claimed in Claim 9, wherein:

the impedance of the capacitor is smaller than the load impedance in the differential signal output apparatus at a transitional response

frequency at which a transitional current flows to the capacitor.

13. A semiconductor integrated circuit apparatus provided with a differential output circuit comprising:

a differential pair constituted by arranging wiring between differential input signals and between differential output signals and arranging transistors symmetrically;

a current source connected to one end of the differential pair and so arranged that connection wiring lines to the transistors be symmetrical; and

a capacitor connected between a branching node for branching connection wiring from the current source to the transistors and a low impedance node and arranged in an area between the transistors.

14. A semiconductor integrated circuit apparatus provided with a differential output circuit comprising:

a differential pair constituted by arranging wiring between differential input signals and between differential output signals and arranging transistors symmetrically;

a first current source connected to one end of the differential pair and so arranged that connection wiring lines to the transistors be symmetrical; and

a capacitor connected between a branching node for branching connection wiring from the first current source to the transistors and a current supply unit having a current supply capacity equal to or greater than the amperage supplied by the first current source and arranged with the same symmetry as the symmetry of arrangement between the transistors.

15. A semiconductor integrated circuit apparatus provided with a differential output circuit comprising:

a first differential pair constituted by arranging wiring between differential input signals and between differential output signals and arranging transistors of a first conductivity type symmetrically;

a first current source connected to one end of the first differential pair and so arranged that connection wiring lines to the transistors of the first conductivity type be symmetrical;

a second differential pair arranged opposite to the first differential pair, constituted by arranging wiring between differential input signals and between differential output signals and arranging transistors of a second conductivity type symmetrically;

a second current source connected to one end of the second differential pair and so arranged that connection wiring lines to the transistors of the second conductivity type be symmetrical; and

a capacitor connected between a first branching node for branching connection wiring from the first current source to the transistors of the first conductivity type and a second branching node for branching connection wiring from the second current source to the transistors of the second conductivity type and arranged in an area surrounded by the first differential pair and the second differential pair.

16. A differential signal transmission system provided with a differential output circuit comprising:

a differential input unit into which differential signals are entered;

a current supply unit for supplying a current to the differential input unit; and

a capacitor connected between a connection node between the differential input unit and the current supply unit and a low impedance node.

17. A differential signal transmission system provided with a differential output circuit comprising:

a differential input unit into which differential signals are entered;

a first current supply unit for supplying a current to the

differential input unit; and

a capacitor connected between a connection node between the differential input unit and the first current supply unit and a second current supply unit having a current supply capacity equal to or greater than the amperage supplied by the first current supply unit.

18. A differential signal transmission system provided with a differential output circuit comprising:

a first differential input unit configured in a first conductivity type for entering differential signals;

a first current supply unit for supplying a current to the first differential input unit;

a second differential input unit configured in a second conductivity type, of which differential output terminals are connected to the differential output terminals of the first differential input unit to receive the differential signals;

a second current input unit for supplying a current to the second differential input unit; and

a capacitor connected between a connection node between the first differential input unit and the first current input unit and another connection node between the second differential input unit and the second current input unit.

19. A signal detection apparatus comprising:

a level detection unit for detecting the voltage amplitude level of input signals;

a state transition detection unit for detecting any state transition in the output signals of the level detection unit;

a signal confirmation unit for issuing a notification signal when the state transition detection unit has detected state transitions a prescribed number of times during a first prescribed length of time;

a non-signal confirmation unit for issuing a notification signal when

the state transition detection unit has detected no state transition during a second prescribed length of time; and

a detect signal generation unit for generating a detect signal that is validated by the signal confirmation unit and invalidated by the non-signal confirmation unit.

20. The signal detection apparatus, as claimed in Claim 19, wherein:

the level detection unit has a comparator comparing, the voltage amplitude level of the input signal with a prescribed voltage.

21. The signal detection apparatus, as claimed in Claim 19, wherein:

the output signals of the level detection unit are logic signals; and

the state transition detection unit, the signal confirmation unit, the non-signal confirmation unit and the detect signal generation unit are configured of logic circuits.

22. The signal detection apparatus, as claimed in Claim 19, wherein:

the state transition detection unit detects as a state transition an output signal supplied from the level detection unit in a prescribed combination of the input signals.

23. The signal detection apparatus, as claimed in Claim 19, wherein:

the state transition is detected on the basis of the transition of the voltage amplitude level of the input signals at above a prescribed voltage or at below a prescribed voltage.

24. The signal detection apparatus, as claimed in Claim 23, wherein:

the state transition is the transition of the voltage of the output signals of the level detection unit.

25. The signal detection apparatus, as claimed in Claim 19, wherein:

the signal confirmation unit comprises:

a first time counter of which start of counting the first prescribed length of time is triggered by a first output signal from the state transition detection unit; and

a detector for detecting, during the period of time counting by the first time counter, output signals of the prescribed number of times

following the first output signal from the state transition detection unit.

26. The signal detection apparatus, as claimed in Claim 19, wherein:

the non-signal confirmation unit comprises:

a second time counter of which start of counting the second prescribed length of time is triggered by an output signal from the state transition detection unit.

27. The signal detection apparatus, as claimed in Claim 19, wherein:

the detect signal generation unit comprises:

a flip-flop of which setting signal is the notification signal from the signal confirmation unit and of which resetting signal is the notification signal from the non-signal confirmation unit.

28. A signal detection method comprising:

a level detection step of detecting the voltage amplitude level of input signals;

a state transition detection step of detecting any state transition in the input signals detected at the level detection step;

a signal confirmation step of notifying the detection of the state transitions a prescribed number of times during a first prescribed length of time at the state transition detection step;

a non-signal confirmation step of notifying the failure to detect the state transition during a second prescribed length of time at the state transition detection step; and

a detect signal generation step of generating a detect signal that is validated at the signal confirmation step and invalidated at the non-signal confirmation step.

29. The signal detection method, as claimed in Claim 28, wherein:

the level detection step includes a comparing step of comparing the voltage amplitude level of the input signal with a prescribed voltage.

30. The signal detection method, as claimed in Claim 28, wherein:

at the state transition detection step, when the input signals are entered in a prescribed combination, the input signals detected at the level

detection step are detected as state transition.

31. The signal detection method, as claimed in Claim 28, wherein:

at the state transition detection step, the state transition is detected on the basis of the transition of the voltage amplitude level of the input signals at above a prescribed voltage or at below a prescribed voltage.

32. The signal detection method, as claimed in Claim 28, wherein:

the signal confirmation step comprises:

a first time counting step of which start of counting the first prescribed length of time is triggered by a first transition of the input signals detected at the state transition detection step; and

a detection step at which, during the period of time counting at the first time counting step, the state transitions of following the input signals detected at the state transition detection step are detected the prescribed number of times.

33. The signal detection method, as claimed in Claim 28, wherein:

the non-signal confirmation step has a second time counting step of which start of counting the second prescribed length of time is triggered by the state transition of the input signals detected at the state transition detection step.

34. A signal transmission system comprising:

a serial bus; and

a signal detection apparatus comprising:

a level detection unit, connected on the serial bus, for detecting the voltage amplitude level of input signals from the serial bus; a state transition detection unit for detecting any state transition in the output signals of the level detection unit; a signal confirmation unit for issuing a notification signal when the state transition detection unit has detected the state transitions a prescribed number of times during a first prescribed length of time; a non-signal confirmation unit for issuing a notification signal when the state transition detection unit has detected no state

transition during a second prescribed length of time; and a detect signal generation unit for generating a detect signal that is validated by the signal confirmation unit and invalidated by the non-signal confirmation unit,

wherein the signal transmission system transmits signals by detection signals on a serial bus by the signal detection apparatus.

35. A signal transmission system for transmitting signals by detection signals on a serial bus by a signal detection method comprising: a level detection step of detecting the voltage amplitude level of input signals on the serial bus; a state transition detection step of detecting any state transition in the input signals detected at the level detection step; a signal confirmation step of notifying the detection of the state transitions a prescribed number of times during a first prescribed length of time at the state transition detection step; a non-signal confirmation step of notifying the failure to detect the state transition during a second prescribed length of time at the state transition detection step; and a detect signal generation step of generating a detect signal that is validated at the signal confirmation step and invalidated at the non-signal confirmation step.

36. The signal transmission system, as claimed in Claim 34, wherein:

the serial bus is a bus either meeting or compliant with the P1394b standard.

37. The signal transmission system, as claimed in Claim 35, wherein:

the serial bus is a bus either meeting or compliant with the P1394b standard.

38. A computer-readable program for executing signal transmission on a serial bus by an input signal detection method comprising:

a level detection step of detecting the voltage amplitude level of input signals;

a state transition detection step of detecting any state transition in the input signals detected at the level detection step;

a signal confirmation step of notifying the detection of the state transitions a prescribed number of times during a first prescribed length of time at the state transition detection step;

a non-signal confirmation step of notifying the failure to detect the state transition during a second prescribed length of time at the state transition detection step; and

a detect signal generation step of generating a detect signal that is validated at the signal confirmation step and invalidated at the non-signal confirmation step.